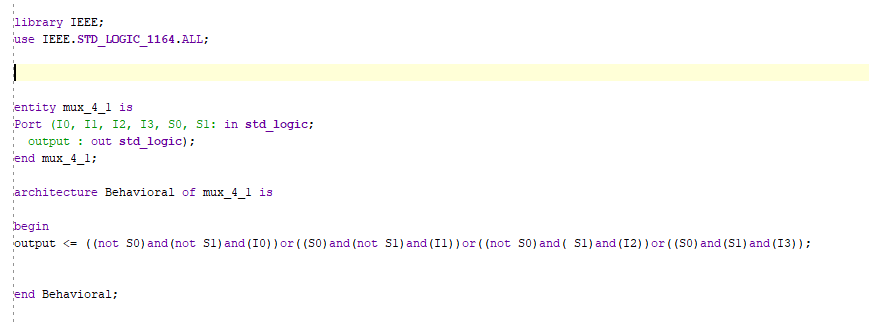
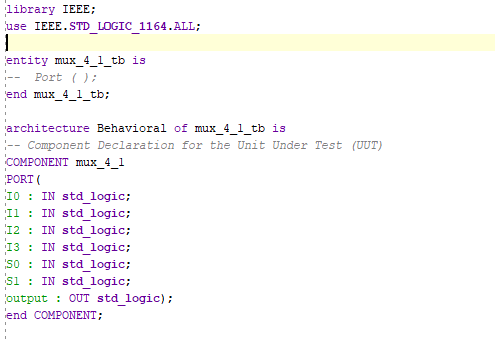
# Task 02 Day 05

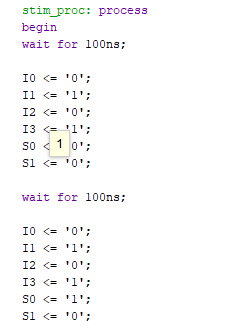
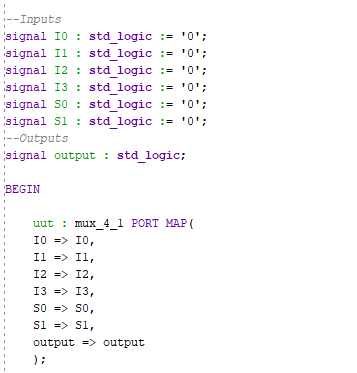
**Team Members:** Rashmi Singh, Ankit Soni, Vishesh Chhaperwal, Amrutha Varshini, Mohan Satwik, Azmeera thrupathi

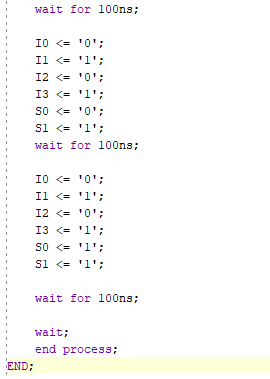
## Verilog Code for 4x1 Mux:



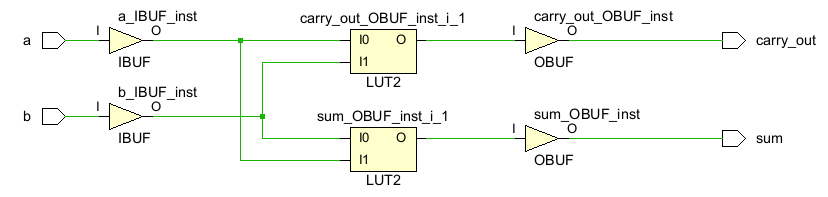
**Test Bench:**



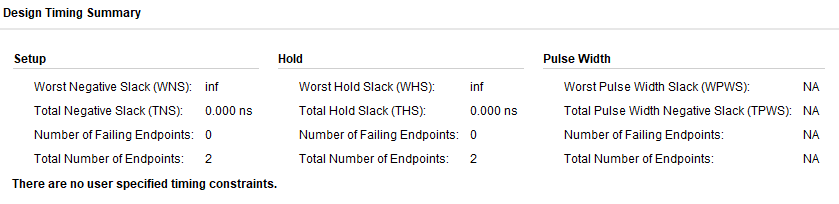




**Schematic Diagram:**



**Design Timing Summary:**



**Device:**

